UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,474	10/25/2001	John E. Barth JR.	FIS920010094US1	5062

32074 7590 05/12/2004

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/035,474	Applicant(s) BARTH ET AL.	
	Examiner John P Trimmings	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 are presented for examination.

Information Disclosure Statement

The examiner acknowledges the applicant's Information Disclosure Citation and has considered the documents listed therein.

Drawings

1. New corrected drawings are required in this application because the present drawings are not of a quality that can be published. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-5, 13-16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka et al., U.S. Patent No. 4918692, in view of Matsumoto et al., U.S. Patent No. 5278839, and further in view of Lee et al., U.S. Patent No. 5748543.

As per Claims 1 and 13:

Hidaka et al. teaches an ECC based circuit and method within an integrated circuit memory for self-repair of a failed memory element therein (column 4 lines 51-58), comprising: processing, within said integrated circuit, data and check bits retrieved from addressed memory locations (Hidaka et al. column 5 lines 16-26); whereby said

failed memory element within said integrated circuit is identified and repaired automatically by circuitry within said integrated circuit (Hidaka et al. column 4 lines 51-55). But Hidaka et al. does not teach recording the faulty locations and identifying and replacing failed elements based on pattern. However, the following references teach these features: Matsumoto et al. teaches in an analogous art, automatically recording locations of memory failures within said integrated circuit based on a fault indicator (column 5 lines 14-29). It would have been obvious to modify the circuit and method of Hidaka et al. by adding the capability as taught by Matsumoto et al. in order to log failures as they occur. And Matsumoto et al., in column 1 lines 1-53 explains that the invention provides a way to further continue repairing faults after installation of a circuit in a system. Also, Lee et al., in the Abstract and in column 3 lines 31-43 teaches using logic circuits within the integrated circuit to automatically identify failure patterns based on said locations (defect indicating signal); and using at least second logic circuits within said integrated circuit (spare substituting circuit) to automatically replace a failed memory element with a redundancy element based on at least one said identified failure pattern. It would have been obvious to additionally modify the circuit and method of Hidaka et al. by adding the failure replacement units taught by Lee et al. into the circuit. Lee et al., in column 2 lines 27-33, also boasts the advantage of repair after device packaging. One with ordinary skill in the art at the time of the invention, motivated as suggested above for both secondary references, would combine all, and so the claims are rejected.

As per Claims 2 and 14:

The method and circuit of claims 1 and 13 wherein said integrated circuit memory is of the type selected from dynamic random access memory (DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory is also taught by Matsumoto et al. in column 1 lines 6-16.

As per Claims 3 and 24:

The method and circuit of claims 1 and 13 wherein said failed memory element is replaced with a redundancy element selected from the group consisting of at least row redundancy element and column redundancy element is further taught by Lee et al. in the Abstract.

As per Claims 4, 5, 15 and 16:

Based on the method and circuit of claims 1 and 13 wherein said electrically alterable circuit connections include at least one selected from the group consisting of electronic fuse and electronic anti-fuse is also taught by Lee et al. in the Abstract.

3. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka et al., U.S. Patent No. 4918692, in view of Matsumoto et al., U.S. Patent No. 5278839, and in view of Lee et al., U.S. Patent No. 5748543 as applied to Claims 2 and 14, and further in view of Hughes et al., U.S. Patent No. 6691252. The method and circuit of claims 2 and 14 wherein said integrated circuit memory is incorporated within an integrated circuit having a microprocessor is taught by Hughes et al. in column 9 lines 59-65. It would have been obvious to modify the circuit of Hidaka et al. to additionally provide failure recovery to embedded memories within a microprocessor.

And Hughes et al., in column 3 lines 55-59 recites an advantage being the capability to repair a fault at the same time testing continues to be executed within the circuit. One with ordinary skill in the art at the time of the invention, motivated by Hughes et al. as suggested, would combine the references, and so the claims are rejected.

4. Claims 11-12 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka et al., U.S. Patent No. 4918692, in view of Matsumoto et al., U.S. Patent No. 5278839, and in view of Lee et al., U.S. Patent No. 5748543 as applied to Claims 2 and 14, and in view of Hughes et al., U.S. Patent No. 6691252 as applied to Claims 10 and 21 above, and further in view of Eaton et al., U.S. Patent No. 4939694.

As per Claims 11 and 22:

The method and circuit of claims 10 and 21 wherein said integrated circuit memory is of the DRAM type and wherein said locations are automatically recorded while said integrated circuit is in a normal operational mode is further taught by Eaton et al. in column 1 lines 15-16 and column 7 lines 1-28. It would have been obvious to modify the circuit and method of Hidaka et al. to include DRAM type memories and testing to occur under normal conditions thereby reducing cost. And in column 2 lines 14-17, Eaton et al. recites the advantage of less costly testing expense as well as improved product yield. And one with ordinary skill in the art at the time of the invention, motivated by Eaton et al., would combine the references, and so the claims are rejected.

As per Claims 12 and 23:

The method and circuit of claims 11 and 22 wherein said failed memory element is automatically replaced when said integrated circuit remains installed within a product for normal use is also taught by Eaton et al. in column 7 lines 43-55. And in view of the motivation above, the claims are rejected.

5. Claims 6, 8, 9 and 17, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka et al., U.S. Patent No. 4918692, in view of Matsumoto et al., U.S. Patent No. 5278839, and in view of Lee et al., U.S. Patent No. 5748543 as applied to Claims 1 and 13 above, and further in view of Eaton et al., U.S. Patent No. 4939694.

As per Claims 6 and 17:

References Hidaka et al., Matsumoto et al., and Lee et al. fail to further teach the method and circuit of claims 1 and 13 wherein said memory failures are automatically recorded, said failure patterns automatically identified, and said failed memory element is automatically replaced while said integrated circuit is in a normal operational mode. In an analogous art however, Eaton et al. does teach this feature in column 7 lines 1-28. It would have been obvious to modify the circuit and method of Hidaka et al. to include DRAM type memories and testing to occur under normal conditions thereby reducing cost. And in column 2 lines 14-17, Eaton et al. recites the advantage of less costly testing expense as well as improved product yield. And one with ordinary skill in the art at the time of the invention, motivated by Eaton et al., would combine the references, and so the claims are rejected.

As per Claims 8 and 19:

References Hidaka et al., Matsumoto et al., and Lee et al. fail to further teach the method and circuit of claims 1 and 13 wherein said locations are automatically recorded while said integrated circuit is in a normal operational mode and wherein said failed memory element is automatically replaced only during a non-normal operational mode of said integrated circuit. Eaton et al. does further teach this optional mode in column 10 lines 11-32. And in view of the motivation previously cited for Eaton et al., the claims are rejected.

As per Claims 9 and 20:

Eaton et al. also teaches the method and circuit of claims 8 and 19 wherein said non-normal operational mode is of a type selected from power-up mode or power-down mode (column 7 lines 38-43). And in view of the motivation previously cited for Eaton et al., the claims are rejected.

6. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka et al., U.S. Patent No. 4918692, in view of Matsumoto et al., U.S. Patent No. 5278839, and in view of Lee et al., U.S. Patent No. 5748543 as applied to Claims 1 and 13 above, and in view of Eaton et al., U.S. Patent No. 4939694 as applied to Claims 6 and 17 above, and further in view of Hotaka, U.S. Patent No. 6442083. Hotaka further teaches the method and circuit of claims 6 and 17 wherein said memory asserts a busy signal during the time that said memory is unavailable for access during which at least one operation is being performed from the group consisting of: identifying said failure patterns and replacing said failed memory element (column 3 lines 65-67, column 4 lines 1-16 and column 6 lines 21-28. It would have been obvious to modify the circuit

and method of Hidaka et al. to assert a busy signal, to an attached microprocessor in one case, when the repair circuit is busy in order to preclude possible conflicts, and to locate repair cells close to the failures for fast repair. And in column 1 lines 53-67 and column 2 lines 1-15 recited the advantage of location redundant cells within the main memory area to reduce chip size, and accommodate repair (speed up repair). And one with ordinary skill in the art at the time of the invention, motivated by Hotaka, would combine references, and so the claims are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100